

Photoflash Capacitor Charger for DSC

Target Spec. REV: 00

General Description

The LD7261A is an ideal charge control IC for flash units with internal soft start, adjustable charging current and output voltage. It provides a proprietary charging algorithm, which charges photoflash capacitor quickly and efficiently. The LD7261A is specially designed for automatically and linearly lowering the charging current at lower battery voltage. As well, a built-in totem pole IGBT driver can drive IGBT quickly and save the board space.

The LD7261A is available in a space-saving MSOP-10 package and is ideal for DSC flash unit.

Features

- Adjustable Charging Current
- Adjustable Output Voltage
- 1.8V~5V Battery Voltage Range
- Internal Soft Start
- Tiny Transformer
- Totem-Pole IGBT Driver

Applications

- DSC Flash Unit
- Film Camera Flash Unit

† Patent pending

Typical Application

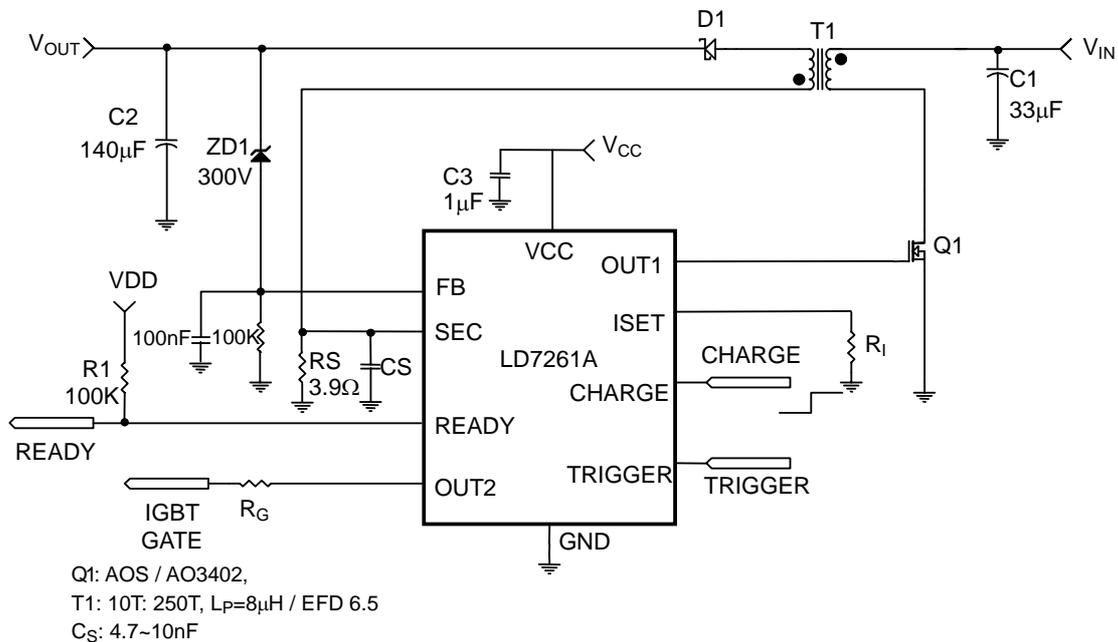
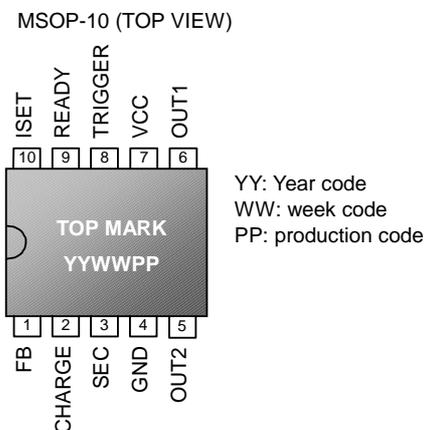


Fig. 1

Pin Configuration

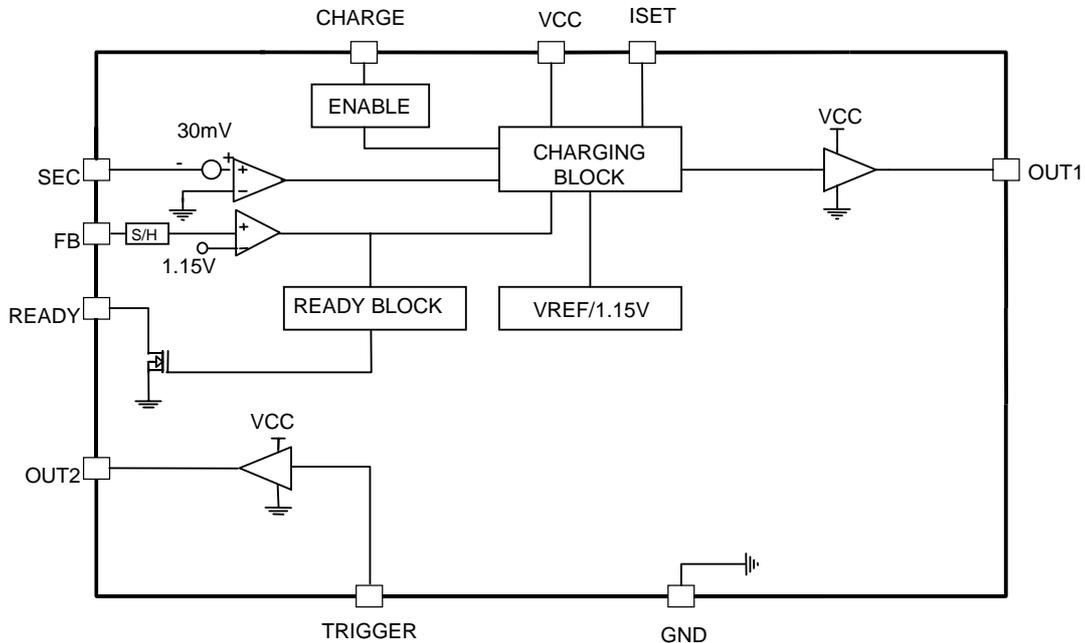


Ordering Information

Part number	Package	Top Mark	Shipping
LD7261APL	MSOP-10 (PB FREE)	7261APL	2500 /tape & reel

Pin Descriptions

PIN	NAME	FUNCTION
1	FB	Output voltage feedback
2	CHARGE	Charging on/off control pin. High=enable low=disable
3	SEC	Secondary winding pin
4	GND	IC GND
5	OUT2	Totem-pole output (IGBT driver)
6	OUT1	Totem-pole output (MOS driver)
7	VCC	Input power of IC
8	TRIGGER	Trigger on/off control pin. High=enable low=disable
9	READY	Charge ready open drain output.
10	ISET	Adjust charging current with R to GND.

Block Diagram

Absolute Maximum Ratings

Supply Voltage Vcc.....	-0.3~6.0V
SEC pin.....	-0.6~(Vcc+0.3) V
FB, Charge, Trigger, ISET pin.....	-0.3~(Vcc+0.3) V
Operating Temperature Range.....	-30°C to 85°C
Storage Temperature Range.....	-55°C to 125°C
Junction Temperature.....	125°C
Lead Temperature (Soldering, 10sec)(LD7261APL).....	260 °C
ESD Level (Human Body Model).....	2KV

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

 (T_A = +25°C unless otherwise stated, V_{CC}=3.3V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Power					
Operating Voltage V _{CC}		2.2		5.5	V
Shutdown Current I _{CC}	Charge=Off, Trigger=Off			1	μA
Nominal Supply Current	V _{CC} =3.3V, D=50%		0.8		mA
FB					
Reference Voltage			1.15		V
Reference Voltage Tolerance				1	%
MOS Driver					
Rising Time	V _{CC} =3.3V, C _L =1nF		40		nS
Falling Time	V _{CC} =3.3V, C _L =1nF		40		nS
IGBT Driver					
Output ON resistor	V _{CC} =3.3V		4	6	Ω
Output OFF resistor	V _{CC} =3.3V		6	9	Ω
Rising Time	V _{CC} =3.3V, C _L =3.9nF		70		nS
Falling Time	V _{CC} =3.3V, C _L =3.9nF		100		nS
ON/OFF					
Trigger On/Off	Enable	1.4			V
	Disable			0.6	V
Charge On/Off	Enable	1.4			V
	Disable			0.6	V
Impedance to GND					
Charge Pin to GND			100K		Ω
Trigger Pin to GND			100K		Ω
Others					
Max Turn On Time	R _i open		7.5		μS
Max Turn On Time Tolerance				6.6	%
SEC Trip Voltage			30		mV
Propagation Delay	(Trigger=High) delay to OUT2		60		nS

Typical Performance Characteristics

$C_{OUT}=140\mu F$

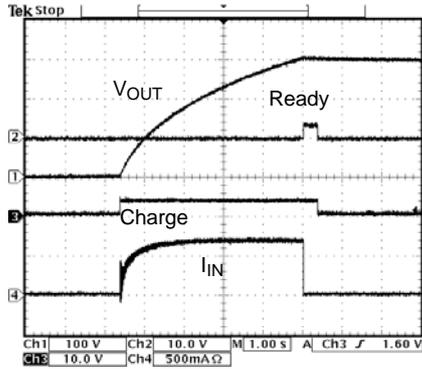


Fig. 2 Charging Waveform $V_{IN}=3V$

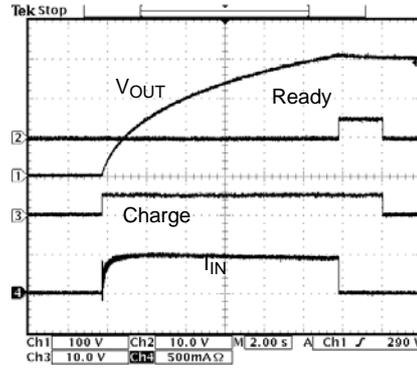


Fig. 3 Charging Waveform $V_{IN}=1.8V$

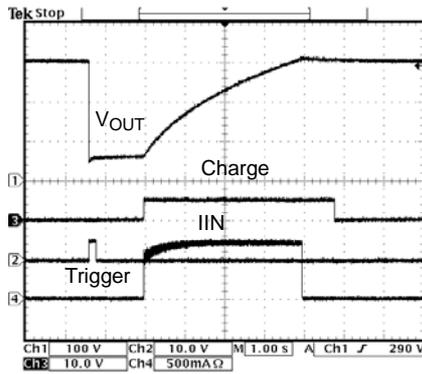


Fig. 4 Charging Waveform $V_{IN}=3V$

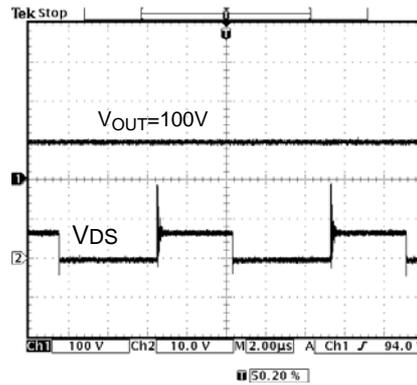


Fig. 5 VDS Waveform

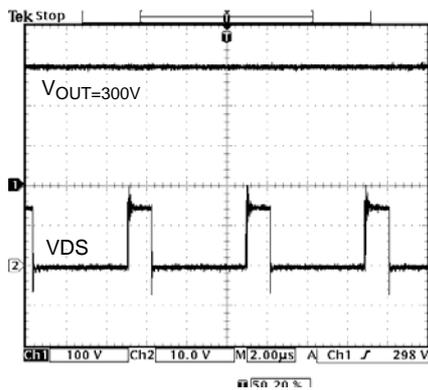


Fig. 6 VDS Waveform

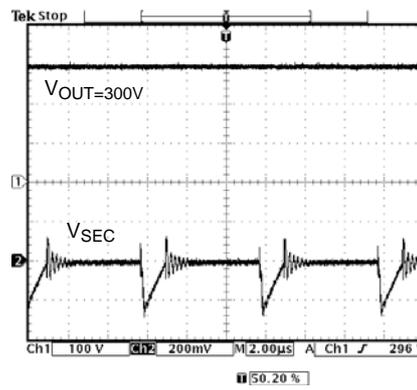


Fig. 7 VSEC Waveform

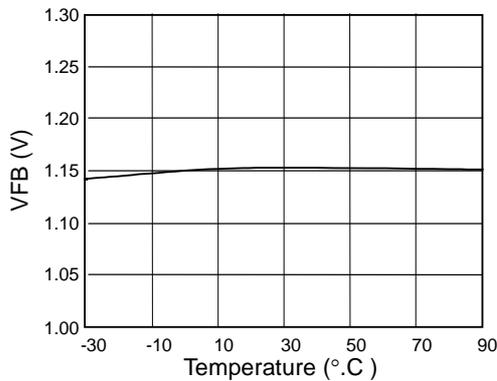


Fig. 8 FB Voltage vs. Temperature

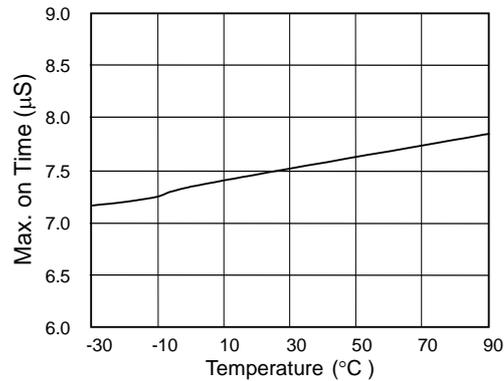


Fig. 9 Max on Time vs. Temperature

Function Description

Adjust Charging Current

The LD7261A provides a flexible way to adjust charging currents.

Just adjust R_I to achieve the desired peak primary charging current.

$$R_I \approx \frac{1.15}{\left(\frac{43 \times V_{BAT}}{L_p \times I_p} - 2.3\right)} M\Omega$$

L_p : primary inductance (μH)

I_p : desired peak primary current (A)

V_{BAT} : battery voltage (V)

Ex: If the desired I_p is 1.6A, $L_p = 8\mu H$, $V_{BAT} = 3.0V$, then

$R_I = 147K/1\%$

Note that the peak primary current must be less than the saturation current of transformer otherwise transformer will be saturated. The LD7261A is designed for linearly lower charging current at lower battery voltage.

The Fig. 10 shows the example of this application.

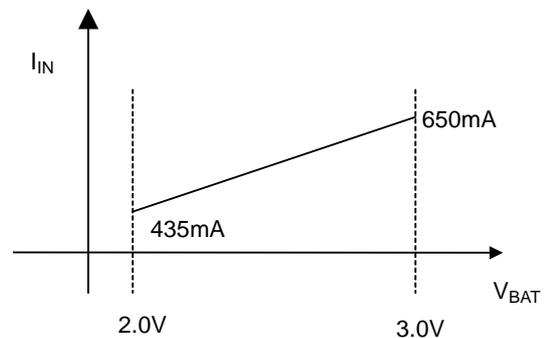


Fig. 10

Acceptable Minimum R_i

The acceptable minimum on time for the LD7261A is

$$T_{ON(min)} \geq 0.52 \left(\frac{V_{out}}{N \times V_{bat min}} + 1 \right) \mu S$$

N : turn ratio of transformer

Ex: $N=25$, $V_{OUT}=300V$, and $V_{BAT(min)}=1.8V$.

$\rightarrow T_{ON(min)} > 4\mu S$

Referring to Fig. 11, it's recommended to choose $R_i > 135K$

($R_i = 1.15V/I_{set}$)

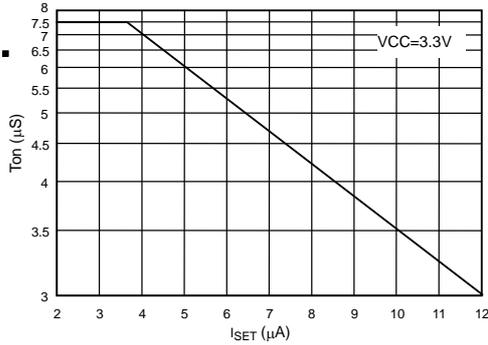


Fig.11

Please always keep R_I value higher than the minimums described above to remain the proper operation in the whole battery range. If the R_I value can't meet the requirement in charging application, please use a larger L_p to adjust the input current lower.

Transformer Selection

A carefully chosen transformer could result in best performance of the LD7261A. Usually, it's suitable to choose a transformer of L_p=8~22µH for V_{BAT} in the voltage range of 1.8V~5V. Also, the turn ratio of the transformer should be considered. Choose it according to the V_{DS} rating of Q1. For example, if V_{DS} rating of Q1 is 30V, then the suitable run ratio is about N=20~25.

Adjust Output Voltage

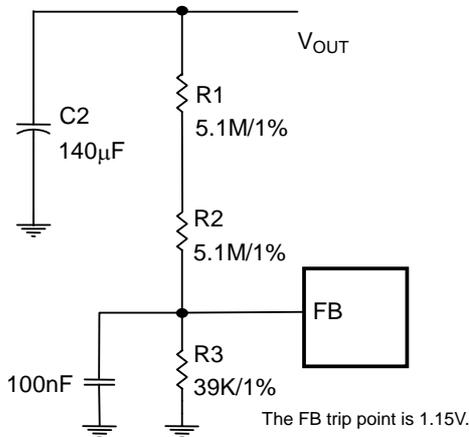


Fig. 12

The LD7261A could sense output voltage by using an output resistor divider. The Fig. 12 shows the application circuit of resistor divider.

$$V_{OUT} = V_{FB} \times (1 + \frac{R1 + R2}{R3})$$

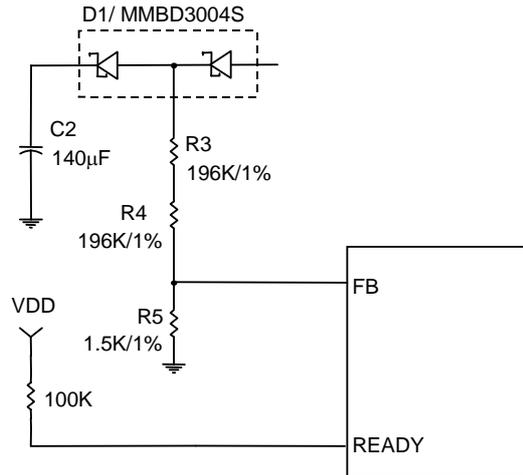


Fig.13

A resistor divider can be connected to the central of the rectifying diode to eliminate the leakage current in the application of Fig. 12 after the charging completes. The Fig. 13 shows the application circuit.

$$V_{OUT} = V_{FB} \times (1 + \frac{R3 + R4}{R5})$$

Choose the lower resistor (R₅ in Fig. 13) connected from FB to GND, less than 2K ohm. Larger resistor combined with parasitic capacitance at FB pin would affect the V_{out} detection accuracy.

Interface

CHARGE, READY and TRIGGER can be easily interfaced to a microprocessor.

The CHARGE pin is the on/off control of charging circuit.

High=enable, Low =disable

The READY pin is an indicator of charging and output voltage state.

High= charging is completed and CHARGE pin is high

Low= otherwise

The TRIGGER pin is the on/off control of the strobe to generate a light pulse.

High=enable, Low =disable

Both of CHARGE pin and TRIGGER pin produce about 100KΩ of impedance to GND, respectively. It's flexible for the user to connect a resistor to increase either the enable or disable level.

Note that the trigger function is only active while the CHARGE pin goes low.

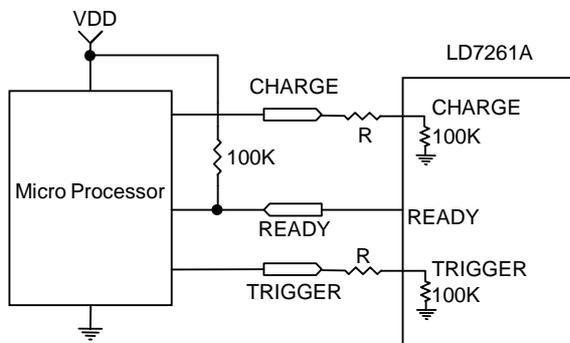
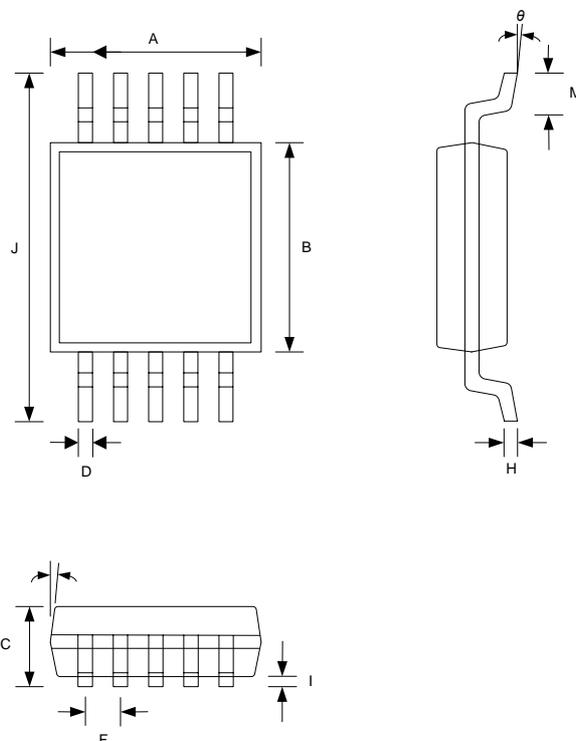


Fig. 14

Layout Consideration

1. The layout of this IC should be far away from any high voltage nodes or paths.
2. Keep the bypass capacitor 1μF very close to IC.
3. Keep output voltage feed back network, R_I , R_S and C_S very close to IC.
4. The Signal ground plane of FB and the SEC pin should be connected to the power ground with a via or only one point to minimize the effect of power ground currents.
4. The Switching node, such as OUT1, should be kept as small as possible and routed away from FB and SEC pin.
5. The PCB traces carrying discontinuous currents and any high current path should be made as short and wide as possible.
6. Please refer to the EV kit for the PCB layout example.

Package Information
MSOP-10


Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	2.896	3.099	0.114	0.122
B	2.896	3.099	0.114	0.122
C	0.813	1.219	0.032	0.048
D	0.152	0.305	0.006	0.012
F	0.470	0.530	0.018	0.020
H	0.127	0.229	0.005	0.009
I	0.051	0.152	0.002	0.006
J	4.699	5.105	0.185	0.201
M	0.406	0.660	0.016	0.026
θ	0°	6°	0°	6°

Important Notice

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