MF426-03a

EPSON

SED17A2 Series

LCD Drivers

Technical Manual

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

CONTENTS

SED1700 Series
Selection Guide

SED1700 Series Selection Guide

■LCD drivers for large-sized displays

High-speed drivers for large-sized dot-matrix displays that complement SEIKO EPSON's dedicated LCD controllers.

SED1700 series

● **Segment drivers**

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Outputs	Data bus	Package	Application
SED1722D0A	4.5–5.5	14Å¦40	1/100 –1/500	80	4-bit parallel	Al pad chip	Used with the SED1733
SED1722F0A						QFP5-100pin	
SED1724D0A					8-bit parallel	Al pad chip	
SED1724F0A						QFP5-100pin	
SED1742D1B	2.7–5.5			160	4-bit parallel	Au bump chip	Used with the SED1743
SED1742T0A						TCP (Outer lead pitch 0.18mm)	
SED1744D1B					8-bit parallel	Au bump chip	
SED1744T0A						TCP (Outer lead pitch 0.18mm)	
SED1748D0B		14–42				Au bump chip	
SED1748T0A						TCP (Outer lead pitch 0.092mm)	
SED1758D0B						Au bump chip	
SED1758T0A						Slim TCP (Outer lead pitch 0.092 mm)	
SED1758T0B						Flex TCP (Outer lead pitch 0.092 mm)	
SED1758T0G						Ultra slim TCP (Outer lead pitch 0.080 mm)	
SED1752T0A				240		Slim TCP (Outer lead pitch 0.070 mm)	
SED1752T0B						Ultra slim TCP (Outer lead pitch 0.070 mm)	
SED17A0T0A*						Ultra slim TCP (Outer lead pitch 0.070 mm)	
SED1756D0A	4.5–5.5	14–40	1/100 –1/400	240	8-bit parallel	Al pad chip (For COG)	Used with the SED1755

* : Under development

● **Common Drivers**

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Outputs	Package	Application
SED1733D0A	4.5–5.5	14–40	1/100 –1/400	100	Al pad chip	
SED1733F0A					QFP5-128pin	
SED1743D1B	2.7–5.5		1/100 –1/500	160	Au bump chip	
SED1743T0A					TCP (Outer lead pitch 0.18mm)	
SED1741D1B		14–42		100	Au bump chip	
SED1741T1B*					TCP	
SED1753D0B				120	Au bump chip	
SED1753T0A					TCP	
SED1755D0A				240	Al pad chip (For COG)	Used with the SED1756

* : Under development

■LCD drivers for grayscale displays

Controlling the lighting time, they avail gray-scale displays in 16 or 64 levels on the LCD panel. The applicable type of panel differs depending on the speed, withstanding voltage and driving method.

● **MIM LCD Drivers**

SED1760 series

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Data bus	Package	Application
SED1765D0A	4.5–5.5	14–40	1/100–1/500	160	–	4-bit parallel x 2	Al pad chip	For MIM-type displays
SED1765D0B							Au bump chip	PWM technology
SED1765T0A							TCP (Outer lead pitch: 0.18mm)	16-level gray
SED1766D0A							Al pad chip	For STN-type displays
SED1766D0B							Au bump chip	PWM technology
SED1766T0A							TCP (Outer lead pitch: 0.18mm)	16-level gray

● **TFT LCD Drivers**

SED1770 series

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment outputs	Data inputs	Package	Application
SED1770D0A	4.5–5.5	5–17	–	160	3 (R,G,B)	Au bump chip	For MIM- or TFT-type displays
SED1771D0A			–	162			

9. SED17A2
LCD Segment Driver

Contents

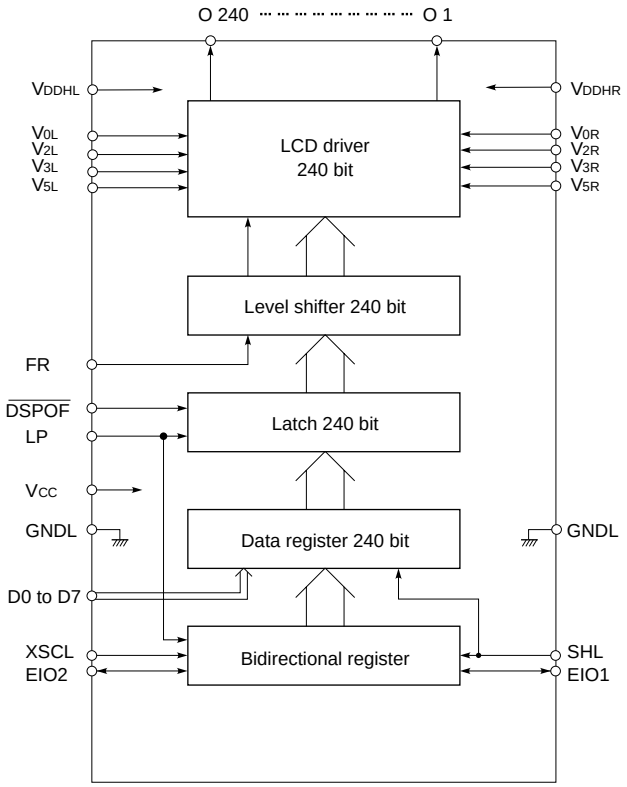
1. OVERVIEW

SED17A2T is a 240-output segment (column) driver suited for large capacity, color STN dot matrix liquid crystal panels. It is used paired with the SED1753.
It is designed for high resolution LCD display, employs high speed enable chain technique for achieving low-power and equips with long type chip layout suited for smaller LCD panels. SED17A2T's low voltage, high speed logic operation capability offers it a wide range of applications.

2. FEATURES

- LCD drive outputs: 240
- Lower operating voltage: 2.7V minimum
- Applicable to high duty drive: 1/500 (for reference)
- Wide LCD drive voltage range:
  +8V to +42V (V_{CC} = 3 to 5.5V)
- High speed and low-power data transfer supported by the 8 bit bus, enable chain approach
  Shift clock frequency …30.0MHz (5V±10%)
  …20.0MHz (3.0V)
  …18.0MHz (2.7V)
- Slimmer chip shape
- Non-bias display off function
- Pin selectable output shift direction
- LCD power bias is offset adjustable according to V_{DDH} or GND level
- Logic operation power: 2.7V to 5.5V
- Package : TCP … SED17A2T**
- This IC is not designed for radiation and light protection

3. BLOCK DIAGRAM



4. BLOCK FUNCTIONS

Enable register

Enable register is a bidirectional register which allows direction select by the SHL input. The shift register output is used for storing the data bus signal to the data register.
As long as the enable signal is disabled, the internal clock signal and data bus are fixed to low-level to introduce the power save mode to the system.
When multiple segment drivers are used, EIO terminals on respective drivers are cascade connected and EIO terminal on the first driver is connected to GND (see the connection example). The enable control circuit automatically detects the end of acquisition of 240 bit of data and transfers the enable signal automatically. Therefore, control signal from the control LSI is no more needed.

Data register

It is a register for converting the data bus signal to and from parallel and serial using the enable shift register output. Therefore, relations between serial display data and segment output is determined independent of number of shift clocks entered.

Latch

Acquires the data register contents at the LP falling edge trigger, then sends it to the level shifter.

Level shifter

A level interface circuit for converting voltage level of a signal from logic system level to LCD drive level.

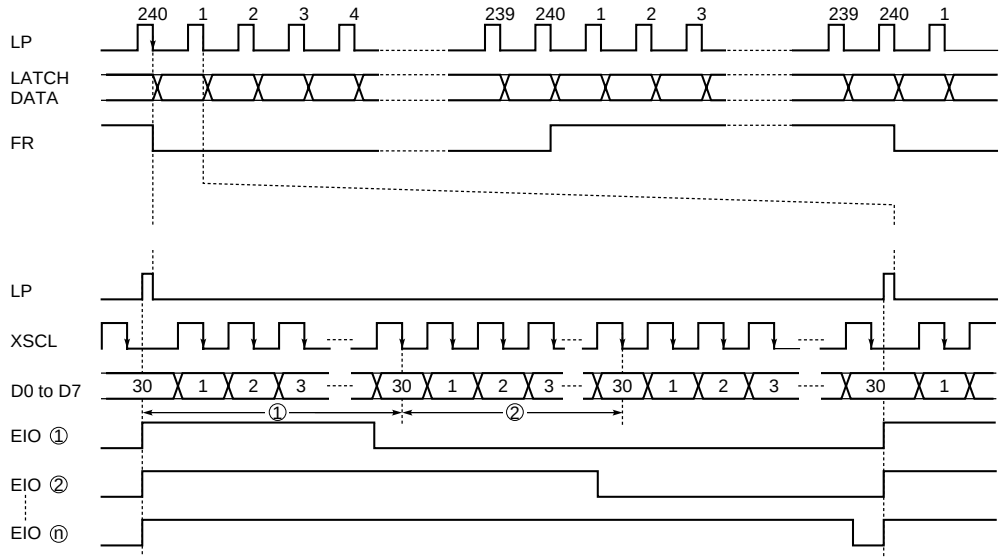
LCD driver

Outputs the LCD drive voltage.
The following table shows relations between data bus signal, frame signal FR and segment output voltage.

$\overline{\text{DSPOF}}$	Data bus signal	FR	Driver output voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	—	V_5

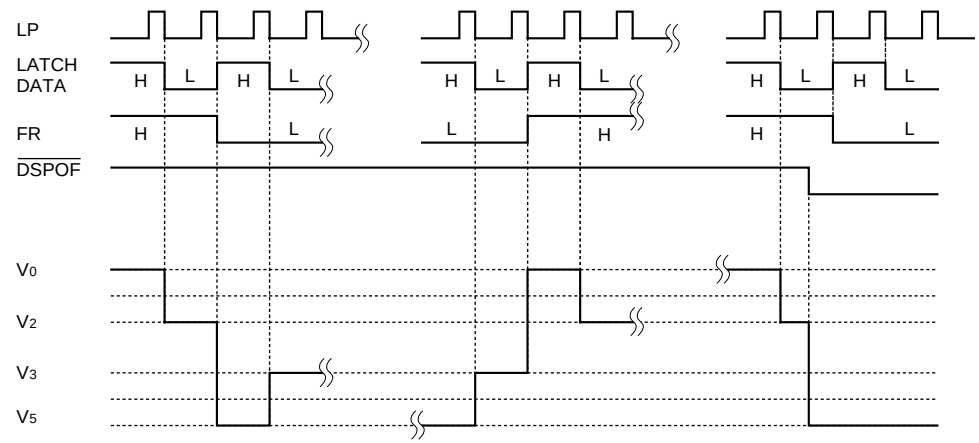
Timing Diagram

Timing Diagram
For 1/240 duty (For reference)



① and ⓝ represent the driver cascade number.

* In high speed data transfer, a longer XSCL cycle must be selected in the LP pulse insertion timing for satisfying the LP→XSCL (t_{LH}) requirement.



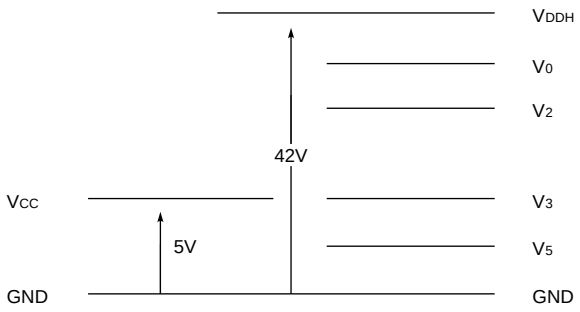
5. PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>No. of pins</th></tr>
<tr><td>O1 to O240</td><td>O</td><td>LCD drive segment (column) output. The output changes at the LP falling edge.</td><td>240</td></tr>
<tr><td>D0 to D3-7</td><td>I</td><td>Display data input</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch pulse input (falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable input or output.
It is set to either input or output depending on the SHL input level. The output is reset as the LP is entered and automatically shifted to low-level as 160 bit of data has been acquired.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and EIO pin I/0 control signal input. The following shows the relation between data and segment output when data is entered to (D0 through D7) pins in the order of F0 through F7 being followed by L0 through and L7.
<table>
<tr><td>F (First), L (last)</td></tr>
</table>
<table>
<tr><td rowspan="2">SHL</td><td colspan="8">O (Output)</td><td colspan="2">EIO</td></tr>
<tr><td>O240</td><td>O239</td><td>O238</td><td></td><td>O3</td><td>O2</td><td>O1</td><td>EIO1</td><td>EIO2</td></tr>
<tr><td>L</td><td>F7</td><td>F6</td><td>F5</td><td>•••</td><td>L2</td><td>L1</td><td>L0</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>L0</td><td>L1</td><td>L2</td><td>•••</td><td>F5</td><td>F6</td><td>F7</td><td>Input</td><td>Output</td></tr>
</table>
Note: Relation between data and segment output is determined independent of number of shift locks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output frame signal input.</td><td>1</td></tr>
<tr><td>V_{CC}, GNDL
GNDR</td><td>Power supply</td><td>Logic operation power GND : 0V V_{CC}: +3.3V, +5V</td><td>3</td></tr>
<tr><td>V_{DDHL}, V_{0L}
V_{2L}, V_{3L},V_{5L},
V_{DDHR}, V_{0R},
V_{2R}, V_{3R}, V_{5R}</td><td>Power supply</td><td>LCD drive circuit power GND : 0V V_{DDH}: +14 to +42V
$V_{DDH} \geq V_0 \geq V_2 \geq 7/9V_0$
$2/9V_0 \geq V_3 \geq V_5 \geq$ GND</td><td>10</td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>Forced bias fixed input.
At low-level, it forces the output to V_5 level.
* This function is not available when the SED17A2T is paired with the SED1703.</td><td>1</td></tr>
</table>

6. ABSOLUTE MAXIMUM RATING

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	GND –0.3 to V_{DDH} +0.3	V
Input voltage	T_I	GND –0.3 to V_{CC} +0.3	V
Output voltage	V_O	GND –0.3 to V_{CC} +0.3	V
EIO output current	I_{OI}	20	mA
Operating temperature	T_{opr}	–30 to +85	°C
Storage temperature	T_{stg}	–55 to +100	°C

Note 1: GND = 0V is assumed for all voltages.
Note 2: Storage temperature assumes that TCP has been mounted.
Note 3: V_0, V_2, V_3 and V_5 voltage must always satisfy $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq GND$.



Note 4: Do not allow the logic operation power goes to floating state or V_{CC} goes to 2.6V or less while LCD drive circuit power is applied. Otherwise, LSI can be permanently damaged. Special care is needed for the system power on or off sequences.

7. ELECTRIC CHARACTERISTICS

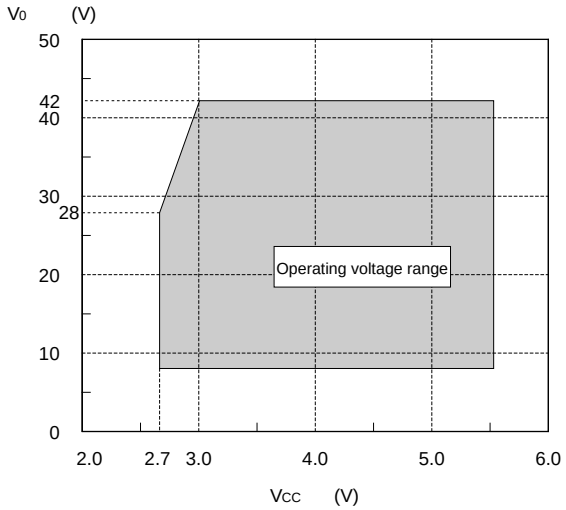
DC Characteristics

Except where otherwise specified, GND = V_5 = 0V, V_{CC} = +5.0V±10% and Ta= –30 to 85°C are assumed.

Items	Codes	Conditions		Min.	Typ.	Max.	Units	Applicable pins
Supply voltage (1)	V_{CC}			2.7	—	5.5	V	V_{CC}
Recommended operating voltage	V_0			14.0	—	40.0	V	V_{0L}, V_{DDHL}
Operatable voltage	V_0	Function		8.0	—	42.0	V	V_{0R}, V_{DDHL}
Supply voltage (2)	V_2	Recommended value		7/9V_0	—	V_0	V	V_{2L}, V_{2R}
Supply voltage (3)	V_3	Recommended value		GND	—	2/9V_0	V	V_{3L},V_{3R}
High level input voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		0.8V_{CC}	—	—	V	EIO1, EIO2, FR D0 to D7, XSCL SHL, LP, $\overline{DSPOF}$
Low level input voltage	V_{IL}			—	—	0.2V_{CC}	V	
High level output voltage	V_{OH}	V_{CC} =	I_{OH} = – 0.6mA	V_{CC} – 0.4	—	—	V	EIO1, EIO2
Low level output voltage	V_{OL}	2.7 to 5.5V	I_{OH} = 0.6mA	—	—	0.4	V	
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		—	—	2.0	µA	D0 to D7, LP, FR XSCL, SHL, $\overline{DSPOF}$
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		—	—	5.0	µA	EIO1, EIO2
Rest current	I_{GND}	V_0 = 14.0 to 42.0V V_{IH} = V_{CC}, V_{IL} = GND		—	—	25	µA	GND
Output resistance	R_{SEG}	ΔVON = 0.5V	V_0 = +36.0V, 1/24	—	0.80	1.1	kΩ	O0 to
		Recommended condition	V_0 = +26.0V, 1/20	—	0.85	1.2	—	O240
Output resistance in-chip deviation	ΔR_{SEG}	ΔVON = 0.5 V_0 = +36.0V, 1/24		—	—	95	Ω	O1 to O240
Mean operating current (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC} V_{IL} = GND, f_{XSCL} = 5.38MHz f_{LP} = 33.6KHz, f_{FR} = 70Hz Input data: Check display, no load		—	0.75	1.7	mA	V_{CC}
		V_{CC} = +3.0V Other conditions are the same as when Vcc = 5V		—	0.3	0.9		
Mean operating current (2)	I_0	V_0 = + 30.0V V_{CC} = +5.0V, V_3 = +4.0V V_2 = +26.0V, V_5 = 0.0V Other conditions are the same as shown in the I_{CC} column		—	0.25	1.4	mA	V_0
Input terminal capacity	C_I	Freq. 1MHz Ta = 25°C		—	—	8	pF	D0 to D7, LP, FR XSCL, SHL, $\overline{DSPOF}$
I/O terminal capacity	$C_{I/O}$	Independent chips		—	—	15	pF	EIO1, EIO2

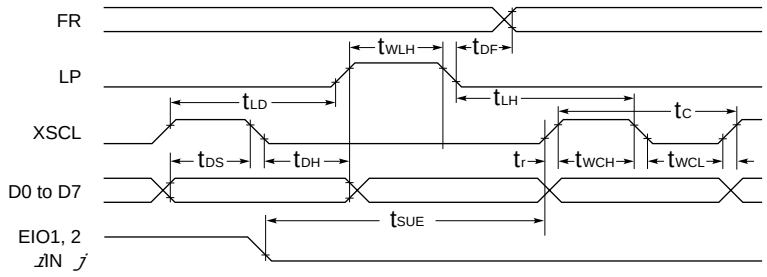
Operating Voltage Range V_{CC}-V_0

V_0 voltage must be selected within the V_{CC}-V_0 operating voltage range as shown below.



AC Characteristics

Input Timing Characteristics



(VCC = +5.0V±10%, Ta = –30 to 85°C)

Items	Codes	Conditions	Min.	Max.	Units
XSCL cycle	t_C	*2	33	—	ns
XSCL high-level pulse width	t_{WCH}		9	—	ns
XSCL low-level pulse width	t_{WCL}	20% and 80% of V_{CC}	9	—	ns
Data setup time	t_{DS}	are assumed for all	5	—	ns
Data hold time	t_{DH}	timing.	5	—	ns
XSCL→LP rise time	t_{LD}		–0	—	ns
LP→XSCLE fall time	t_{LH}		25	—	ns
LP high-level pulse width	t_{WLH}	*1	15	—	ns
Allowable FR delay time	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		5	—	ns
Input signal change time	t_{r1}, t_{f1}	*3	—	50	ns
DSPOF signal change time	t_{r2}, t_{f2}		—	100	ns

(VCC = +2.7V to 4.5V, Ta = –30 to 85°C)

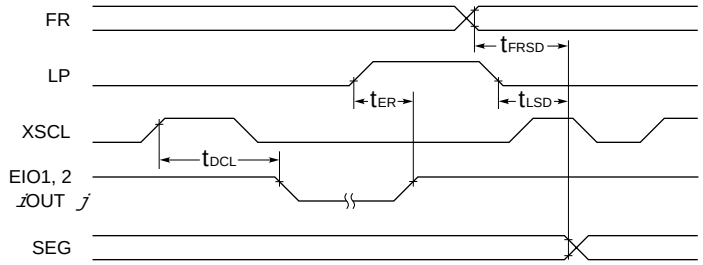
Items	Codes	Conditions	Min.	Max.	Units
XSCL cycle	t_C	VCC = 3.0 to 4.5V	50	—	ns
		*2	55	—	ns
XSCL high-level pulse width	t_{WCH}		15	—	ns
XSCL low-level pulse width	t_{WCL}	20% and 80% of V_{CC}	15	—	ns
Data setup time	t_{DS}	are assumed for all	10	—	ns
Data hold time	t_{DH}	timing.	10	—	ns
XSCL→LP rise time	t_{LD}		–0	—	ns
LP→XSCLE fall time	t_{LH}		30	—	ns
LP high-level pulse width	t_{WLH}	*1	25	—	ns
Allowable FR delay time	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		10	—	ns
Input signal change time	t_{r1}, t_{f1}	*3	—	50	ns
DSPOF signal change time	t_{r2}, t_{f2}		—	100	ns

*1: t_{WLH} regulates high-level period of LP and low-level period of XSCL if LP is entered while XSCL is at low-level.

*2: High speed shift clock (XSCL) operation is regulated by the condition $t_r+t_f \le (t_C-t_{WCL}-t_{WCH})$.

*3: When high speed data transfer is done with continuous shift clock, maximum of the LP signal t_r+t_f is $(t_C+t_{WCH}-t_{LD}-t_{WLH}-t_{LH})$.

Output Timing Characteristics



(V_{CC} = +5.0V±10%, V_0 = +14.0 to 42.0V)

Items	Codes	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	CL (EIO) = 15pF	—	50	ns
EIO output delay time	t_{DCL}		—	25	ns
LP→SEG output delay time	t_{LSD}	CL (On) = 100pF	—	200	ns
FR→SEG output delay time	t_{FRSD}		—	400	ns

(V_{CC} = +2.7V to 4.5V, V_0 = +14.0 to 28.0V)

Items	Codes	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	CL (EIO) = 15pF	—	80	ns
EIO output delay time	t_{DCL}		—	50	ns
LP→SEG output delay time	t_{LSD}	CL (On) = 100pF	—	400	ns
FR→SEG output delay time	t_{FRSD}		—	800	ns

8. LCD DRIVE POWER SUPPLY

Setting up different voltage levels

When setting up respective voltage levels for LCD drive, the best way would be to resistively divide the potential between V_0-GND by means of voltage follower using an operation amplifier. In consideration of the case of using an operation amplifier, the LCD driving minimum potential V_5 and GND are separated and independent terminals are used.

However, since efficacy of the LCD driving output driver deteriorates when the potential of V_5 goes up beyond the GND potential, the potential difference between V_5-GND must always be kept at 0V to 2.5V.

When a resistance exists in series in the V_0 (GND) power supply line, I0 at signal changes causes voltage drop at V_0 (GND) of the LSI supply terminals disabling it to maintain the relations with the LCD potentials of ($V_{DDH} = V_0 \geq V_2 \geq V_3 \geq V_5 \geq$ GND). This could result in permanent damage of the LSI.

When a protective resister is employed, the voltage must be stabilized using an appropriate capacitance.

Precautions for turning power on or off

Since the LCD drive voltage of these LSIs are high, if a voltage of 30V or above is applied to the LCD drive circuit when the logic operation power is floating, the V_{CC} is lowered to 2.6V or less or LCD drive signals are output before applied voltage to the LCD drive circuit is stabilized, excess current flows through possibly damaging the LSI.

It is therefore suggested to maintain the potential of the LCD drive to V_5 level until the LCD drive circuit power is stabilized. Use the display off function ($\overline{DSPOF}$) for this purpose.

Maintain the following sequences when turning power on or off.

When turning power on: Turn on the logic operation power → turn on the LCD drive power or turn them on simultaneously.

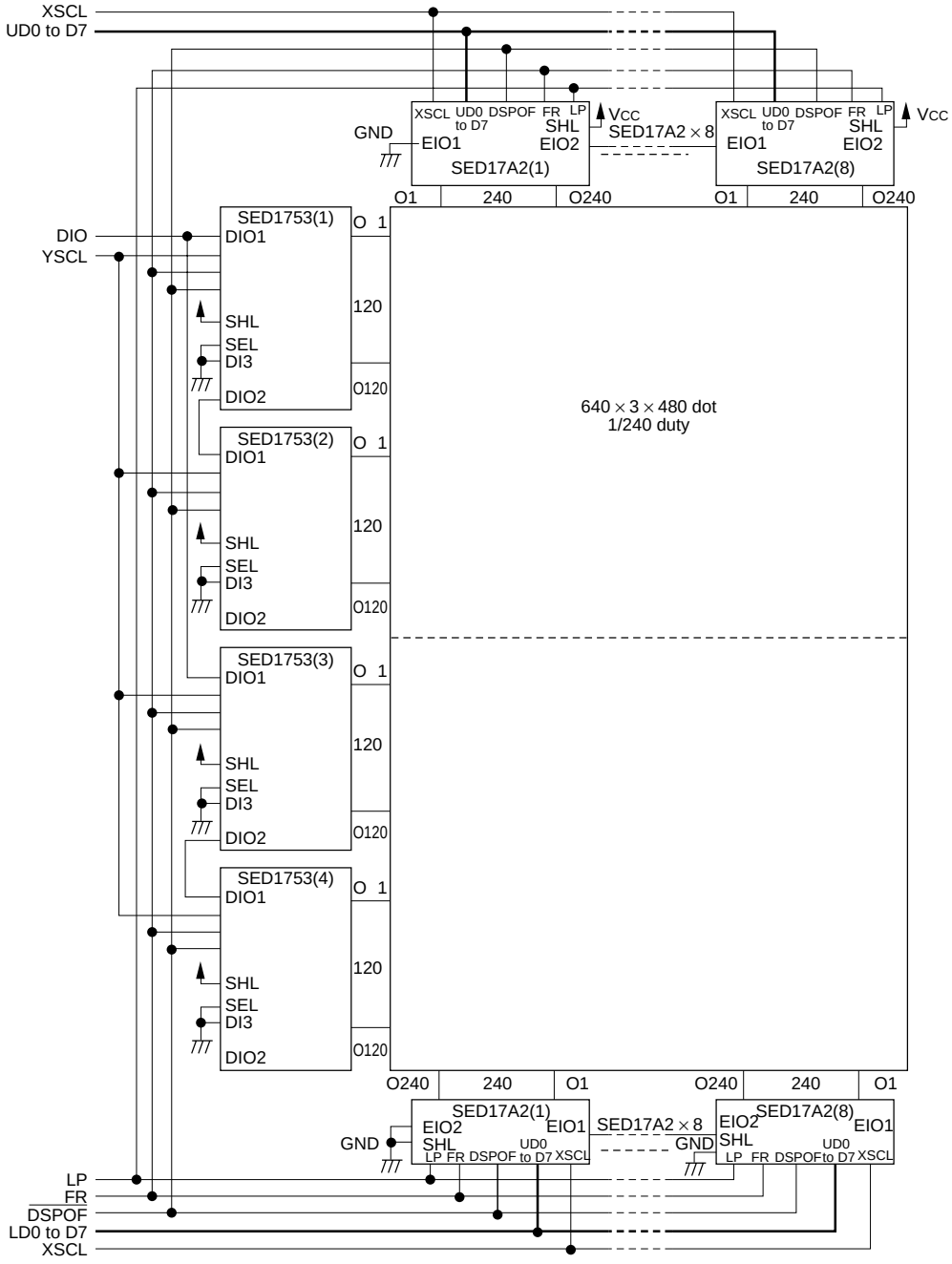
When turning power off: Turn off the LCD drive power → turn off the logic operation power or turn them off simultaneously.

As a protection against excess current, insert a quick melting fuse in series in the LCD drive power line.

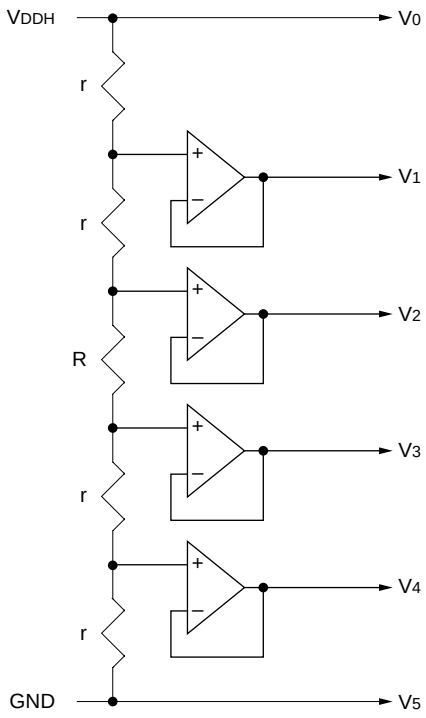
When using a protective resistor, an optimum resistance value must be selected considering the capacitance of the liquid crystal cells.

9. SAMPLE CIRCUIT

Large Screen LCD Structural Diagram



A Sample LCD Power Supply



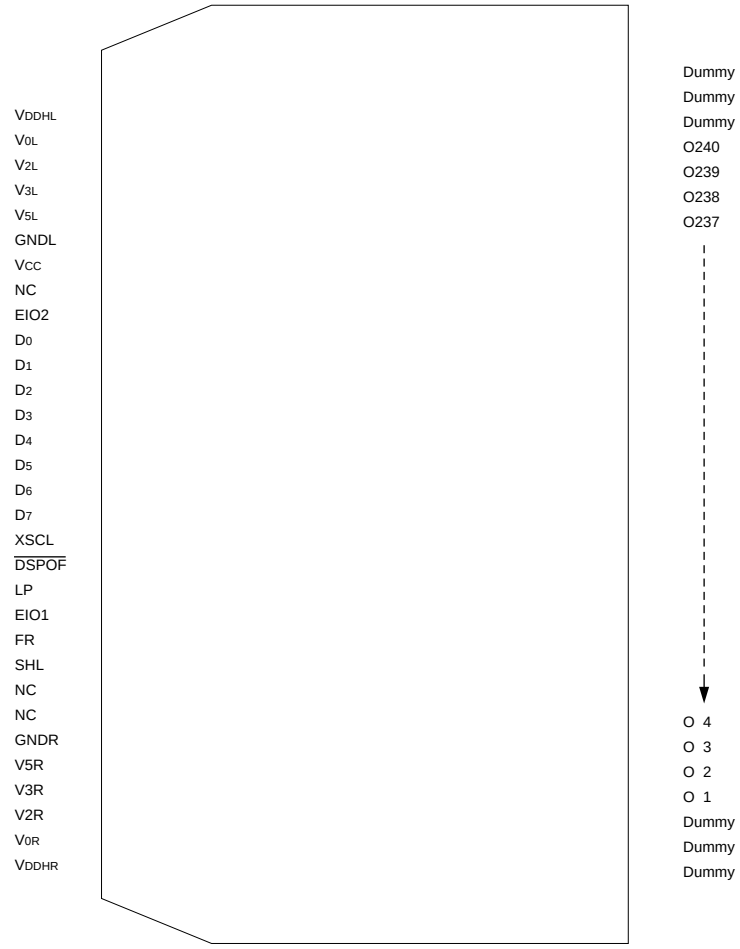
- Smoothing capacitance must be added to the LCD drive power (V_0-V_5) at an appropriate position on the LCD module.
- V_0, V_1, V_4 and V_5 supply power to the SED1753 and V_0, V_2, V_3 and V_5 are used supplying power to the SED17A2T.
- Supplies logic operation voltage to respective ICs.
- Bias capacitors must be installed to appropriate positions between GND-V_{CC} and GND-V_{DDH} for stabilizing voltage and, thus, to provide protection against noise.

  The high tension resistant power (GNDR, GNDL) line might as well be separated from that for the logic operation power (GND) line.

10. TCP

Sample SED17A2T** TCP Pin Layout

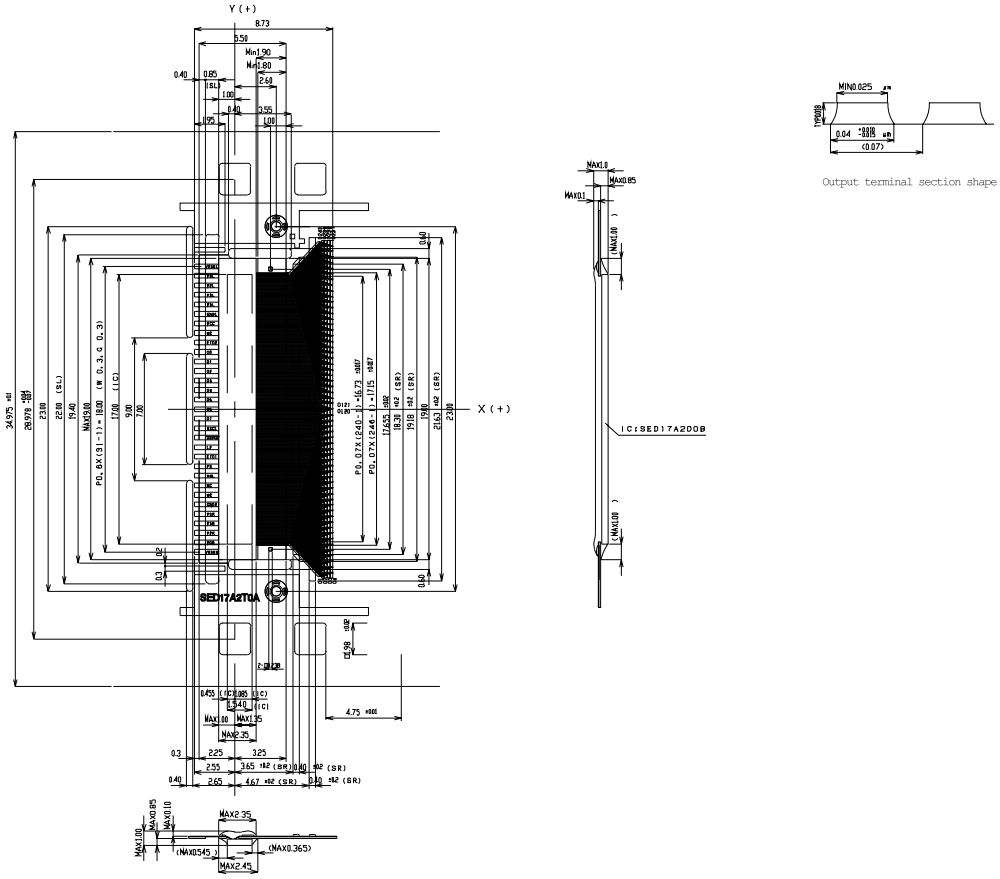
Note: It is not intended to regulate contour of TCP.



11. DIMENSIONAL OUTLINE DRAWING

SED17A2T0A

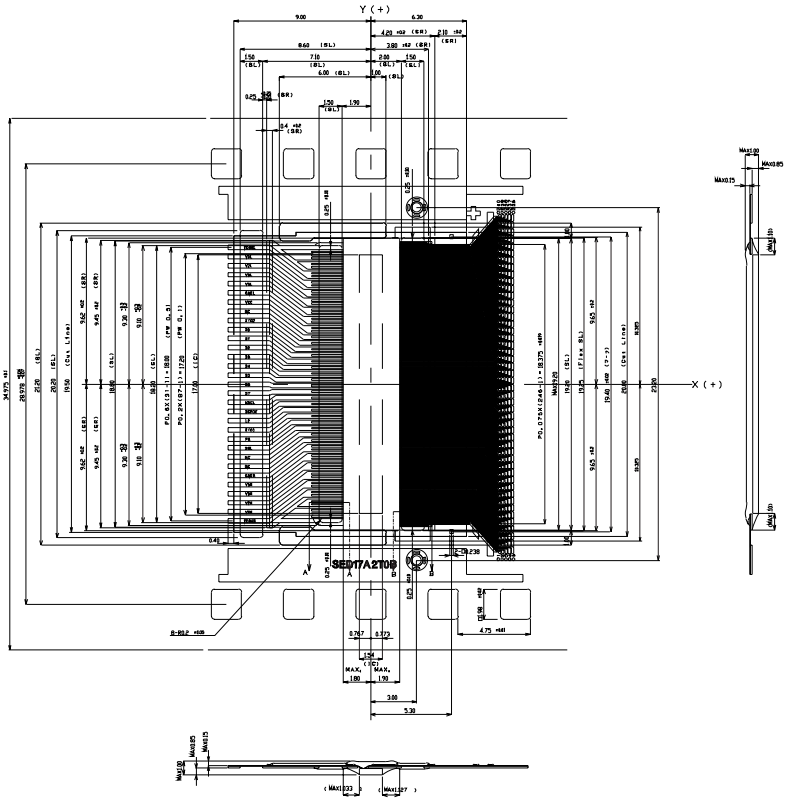
For reference

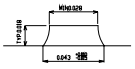


Unit: mm

SED17A2T0B

For reference



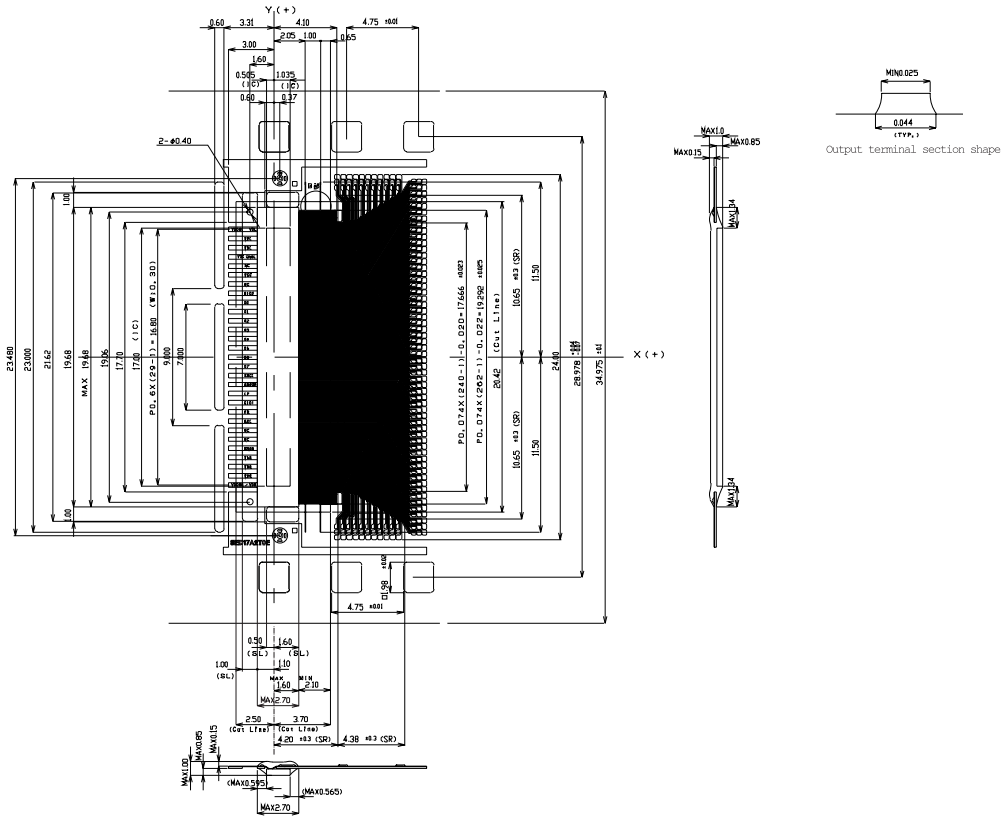


Output terminal section shape

Unit: mm

SED17A2T0E

For reference



Unit: mm