PIXELPLUS CO., LTD.

Preliminary
Data sheet

1/4 inch NTSC/PAL/VGA Single Chip CMOS Image Sensor with 682 X 504 Pixel Array

PC1030K

Rev 0.1

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1/4 inch NTSC/PAL/VGA Single Chip CMOS Image Sensor with 682 X 504 Pixel Array

▶ Features

▷ 682 x 504 total pixel array with RGB bayer color filters and micro-lens and optical black pixel.

▷ Power supply :
AVDD : 2.8V, DVDD : 1.5/1.8V, HVDD : 1.5 ~ 3.3V

▷ Output formats :
CVBS (NTSC/PAL),
ITU-R. BT601/656(60 fields/sec. interlaced @ 27MHz) with CVBS,
320x240(288) YCbCr422 concurrent with CVBS (30(25) frames/sec. @ 27MHz),
Bayer 640x480 (Max. 60 frames/sec. progressive @ 27MHz),
VGA YCbCr422 (Max. 60 frames/sec. progressive @ 54MHz)

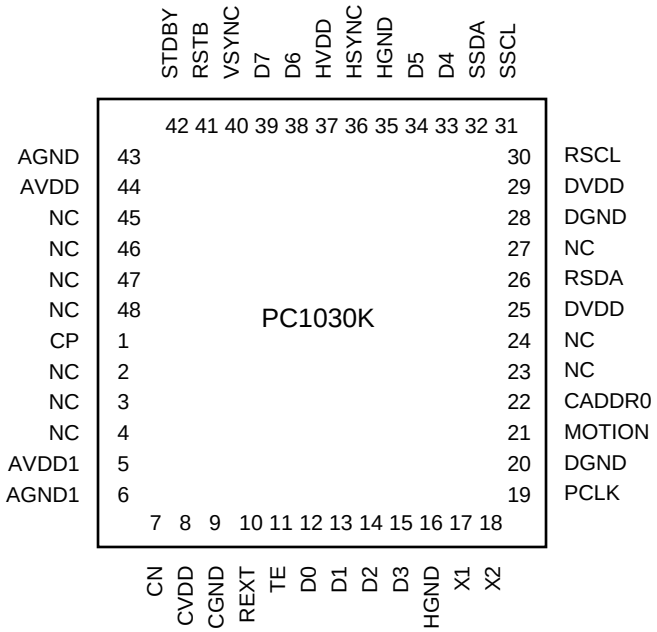
▷ Image processing on chip :
lens shading, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, brightness, contrast, saturation, auto black level compensation, auto white balance, auto exposure control and back light compensation.

▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus.

▷ VGA / QVGA / QQVGA / CIF / QCIF Scaling.

▷ 50Hz, 60Hz flicker automatic cancellation.

▷ High Image Quality and High low light performance.



[Fig. 1] PIN Description (CLCC)

Total Pixel Array	648 x 488
Pixel Size	5.5 um x 5.5 um
Effective Image Area	2.361mm x 1.785 mm
Clock Frequency	27 MHz @ CVBS Max. 54 MHz @ Digital
Frame Rate	60 fields/sec. @ CVBS Max. 60 fps @ Digital
Dark Signal	TBD [mV/sec]
Sensitivity	TBD [V/Lux.sec]
Saturation Level	TBD [mV]
Power Consumption	TBD [mW] @ Dynamic
	TBD [uW] @ Standby
Operating Temp. (Fully Functional Temp.)	TBD
Dynamic Range	TBD [dB]
SNR	TBD [dB]

[Table 1] Typical Parameters

1/4 inch NTSC/PAL/VGA Single Chip CMOS Image Sensor with 682 X 504 Pixel Array

▶ PIN Descriptions

PIN No.	Name	I/O Type	Functions / Descriptions
1	CP	O	Composite Differential Positive signal. (75ohm single termination, 37.5ohm double termination)
2	N.C		
3	N.C		
4	N.C		
5	AVDD1	P	Analog Power supply : 2.8V DC with 0.1uF capacitor to AGND.
6	AGND1	P	Analog Power ground (capacitor ground)
7	CN	O	Composite Differential Negative signal. (75ohm single termination, 37.5ohm double termination)
8	CVDD	P	DAC Power supply : 2.8V DC with 0.1uF capacitor to AGND.
9	CGND	P	DAC Power ground.
10	REXT	I	External Resistor (60k ohm)
11	TE	I	Chip Test Mode enable. Connected to DGND for normal operation
12	DO0	O	Bit 0 of data output.
13	DO1	O	Bit 1 of data output.
14	DO2	O	Bit 2 of data output.
15	DO3	O	Bit 3 of data output.
16	HGND	P	I/O Power ground. This pin can tied with DGND.
17	X1	I	Master clock input pad or Crystal input pad
18	X2	O	Crystal output pad
19	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity and drivability can be controlled anyway.
20	DGND	P	Digital Power ground.
21	MOTION	O	Motion detection. It lets user or processor know whether there are motion of something on video. When the motion exists on the video, the output goes LOW to HIGH
22	CADDR0	I	Chip address bit 0. Chip address can be changed If this CADDR0 Input pin is tied to HVDD or HGND.
23	N.C		
24	N.C		
25	DVDD	P	Digital Power supply : 1.8V DC with 0.1uF to DGND
26	RSDA	I/O	2-wire serial interface master databus. For using external EEPROM
27	N.C		
28	DGND	P	Digital Power ground.

Pin No.	Name	I/O Type	Functions / Descriptions
29	DGND	P	Digital Power ground.
30	RSCL	O	2-wire serial interface master clock input. For using external EEPROM
31	SSCL	I	2-wire serial interface slave clock input.
32	SSDA	I/O	2-wire serial interface slave databus.
33	DO4	O	Bit 4 of data output.
34	DO5	O	Bit 5 of data output.
35	HGND	P	I/O Power ground.
36	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
37	HVDD	P	I/O Power supply: 1.8~3.3V DC with 0.1uF capacitor to HGND.
38	DO6	O	Bit 6 of data output.
39	DO7	O	Bit 7 of data output.
40	VSYNC	O	Vertical sync : Indicates the start of a new frame.
41	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
42	STDBY	I	Power standby mode. When STDBY='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<7:0> and PCLK, HSYNC, VSYNC pins can be programmed to tri-state or all '1' or all '0'. But it is possible to control internal registers through I2C bus interface in STDBY mode. All registers retain their current values.
43	AGND	P	Analog Power ground.
44	AVDD	P	Analog Power supply : 2.8V DC with 0.1uF capacitor to AGND.
45	N.C		
46	N.C		
47	N.C		

[Table 2] Pin Descriptions

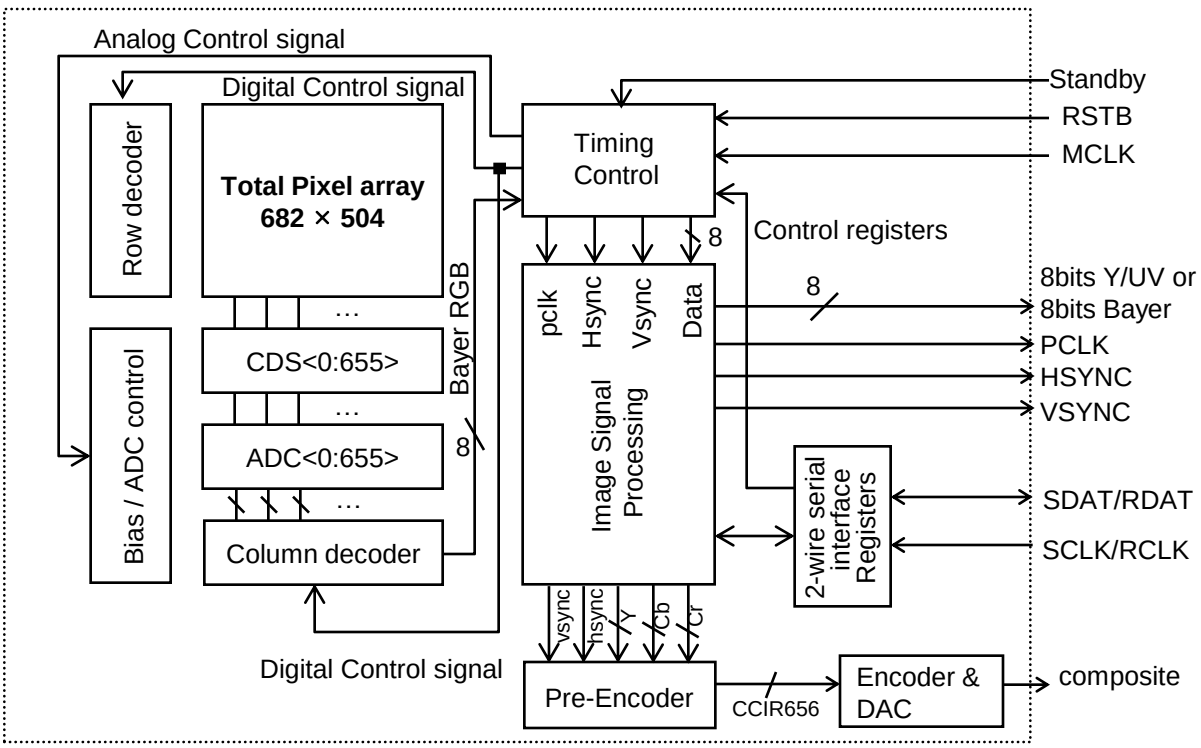
1/4 inch NTSC/PAL/VGA Single Chip CMOS Image Sensor with 682 X 504 Pixel Array

▶ *Signal Environment*

PC1030K has 3.3V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 3.3V. PC1030K input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

▶ *Chip Architecture*

PC1030K has 682 x 504 total pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing block and pre-encoder and encoder blocks to produce YCbCr 4:2:2 output data or composite output. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



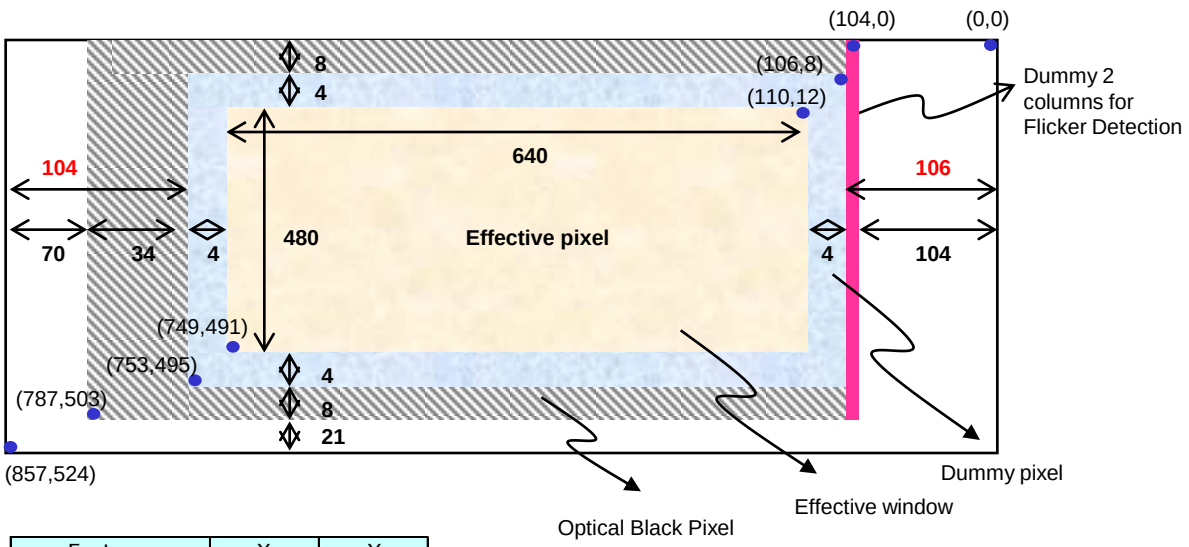
[Fig. 2] Block Diagram

1/4 inch NTSC/PAL/VGA Single Chip CMOS Image Sensor with 682 X 504 Pixel Array

▶ Frame Structure and Windowing

Origin *(0, 0)* of the frame is at the upper right corner. Size of the frame is determined by two registers : *framewidth(Reg.A-06h, A-07h)* and *frameheight(Reg.A-08h, A-09h).* One frame consists of *framewidth + 1* columns and *frameheight + 1* rows. *framewidth* and *frameheight* can be programmed to be larger than total array size. Default window array of 640 x 480 pixels is positioned at *(110, 12).* It is possible to define a specific region of the frame as a window. Pixel scanning begins from *(0, 0)* and proceeds row by row downward, and for each line scan direction is from right to the left. Hsync signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *frameheight* , and 0 to *framewidth* respectively. The counter values increase at the pace of pixel clock (PCLK), which does not change as the frame size is altered. The pixel data rate is fixed and is independent of frame size(frame rate).

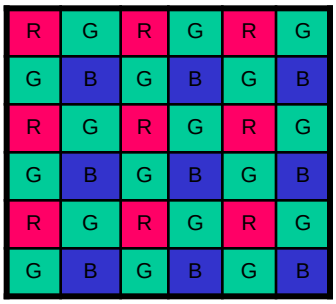
PC1030K NTSC Frame Structure



Features	X	Y
Total Pixels	682	504
Effective Pixels	648	488
OBP pixels	34	16

[Fig. 3] Default data structure of frame and window. (Top view)

▶ *Digital Data Formats*



[Fig. 4] Bayer Color filter pattern

Pixel array is covered by Bayer color filters as can be seen in the [Fig. 4]. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PC1030K provides this Bayer pattern RGB data through an 8bit channel. It takes one PCLK to pass one pixel RGB data to output bus. But one pixel of bayer RGB is composed of one of the 3 components. Therefore the other two components of a pixel must be derived from neighbor pixels. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors.

This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PC1030K adopts a low pass filter to prevent the interference patterns (called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. And then the pixel data pass image processing block to improve the image quality.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$Cb = -0.148R - 0.291G + 0.439, \quad Cr = 0.439R - 0.368G - 0.071B$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

Cb1	Y1	Cr1	Y2	Cb3	Y3	Cr3	Y4	…

[Fig. 5] 4:2:2 YCbCr data sequence.

PC1030K supports 4:2:2 YCbCr data format where Cb and Cr components are horizontally sub-sampled such that U and V for every other pixel are omitted. PC1030K also support 4:2:2 YUV data format.

▶ 2-wire Serial Interface Description

The registers of PC1030K are written and read through the 2-wire Serial Interface. The PC1030K has 2-wire Serial Interface slave. The PC1030K is controlled by the Register Access Clock (SCLK), which is driven by the 2-wire Serial Interface master. Data is transferred into and out of the PC1030K through the Register Access Data (SDAT) line. The SCLK and SDAT lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The 2-wire Serial Interface protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a 2-wire Serial Interface device consists of 7-bit of address and 1-bit of direction. A '0' in the LSB of the address indicates write mode, and a '1' indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The SCLK pulse is provided by the master. The data must be stable. During the HIGH period of the SCLK : it can only change when the SCLK is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

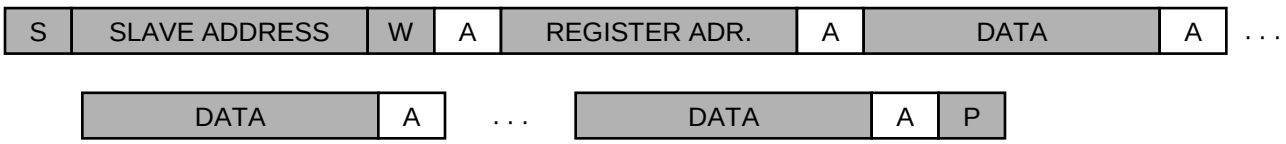
Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master. If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PC1030K uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit. A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

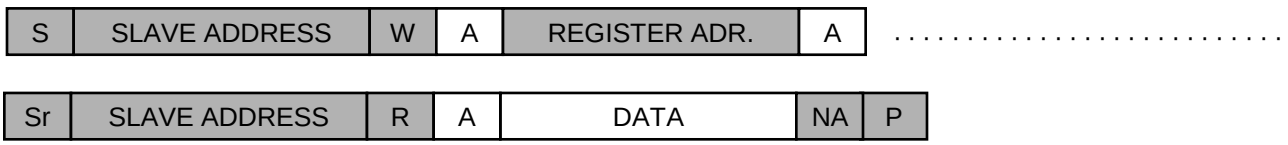
▶ 2-wire Serial Interface Functional Description

Single Write Mode operation

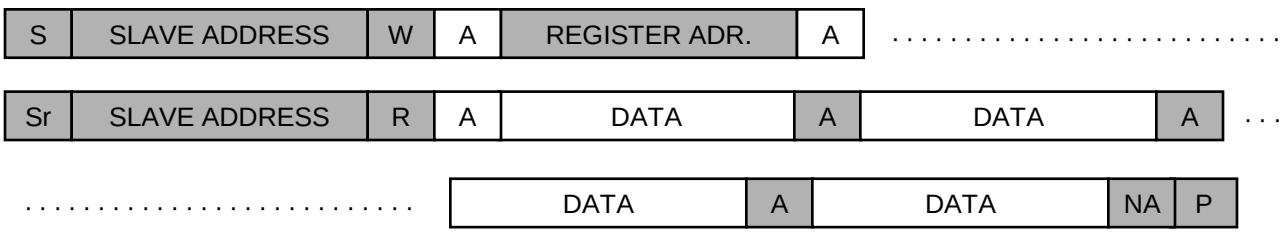
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



From master to slave From slave to master

S: Start condition. Sr : Repeated Start (Start without preceding stop.)

SLAVE ADDRESS: It can be extended 64h to 67h via CADDR0 pad

CADDR0	0	1
write address	64h	66h(default)
read address	65h	67h(default)

R/W: Read/Write selection. High = read / LOW = write.
A: Acknowledge bit. NA : No Acknowledge.
DATA: 8-bit data
P: Stop condition

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.